

Fig. 1

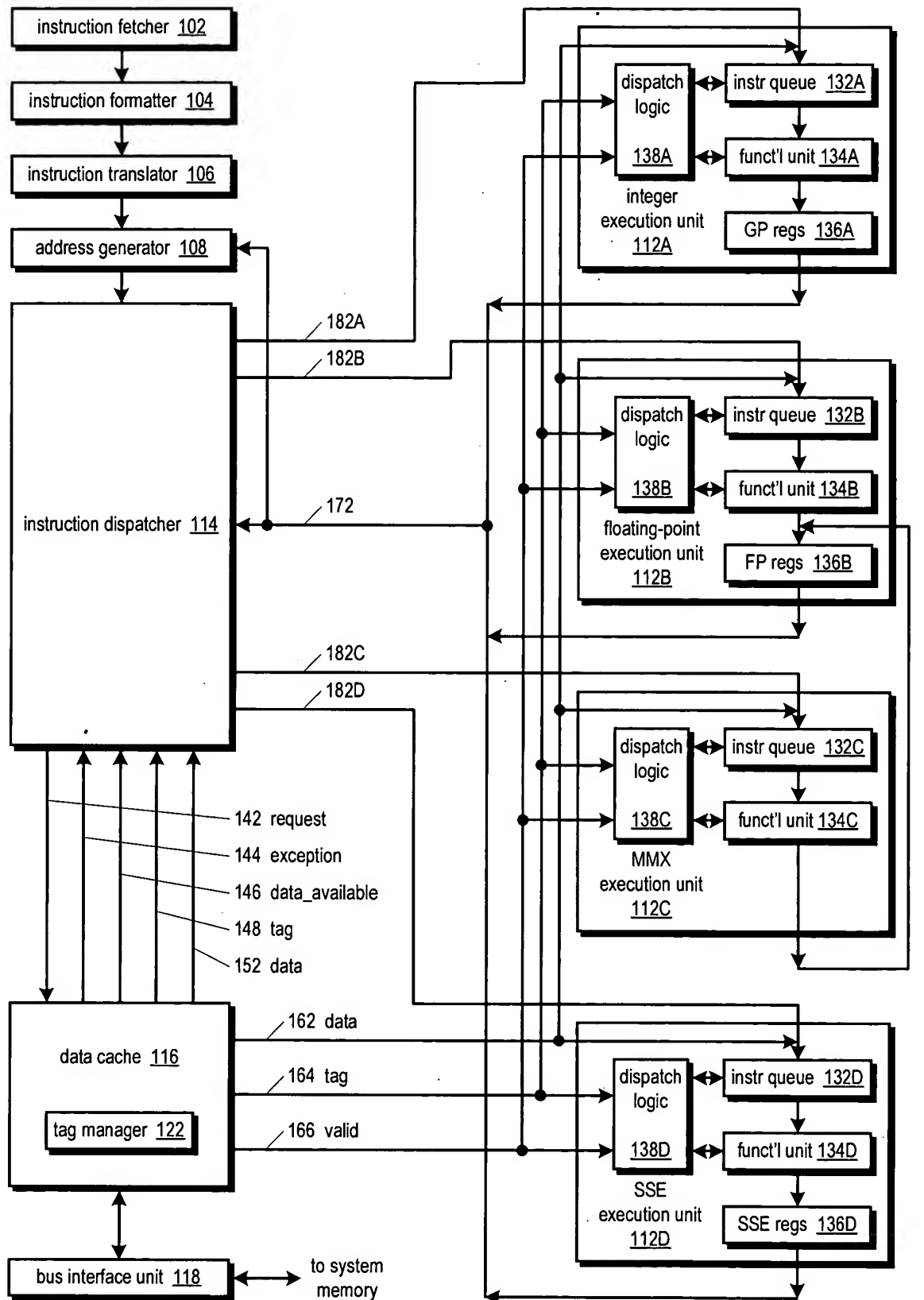
Microprocessor

Fig. 2

Instruction Queue

data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>
data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>
data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>
data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>
data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>
data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>
data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>
data <u>202</u>	DV <u>204</u>	tag <u>206</u>	instruction <u>208</u>	IV <u>212</u>

222 queue entry

132

Fig. 3

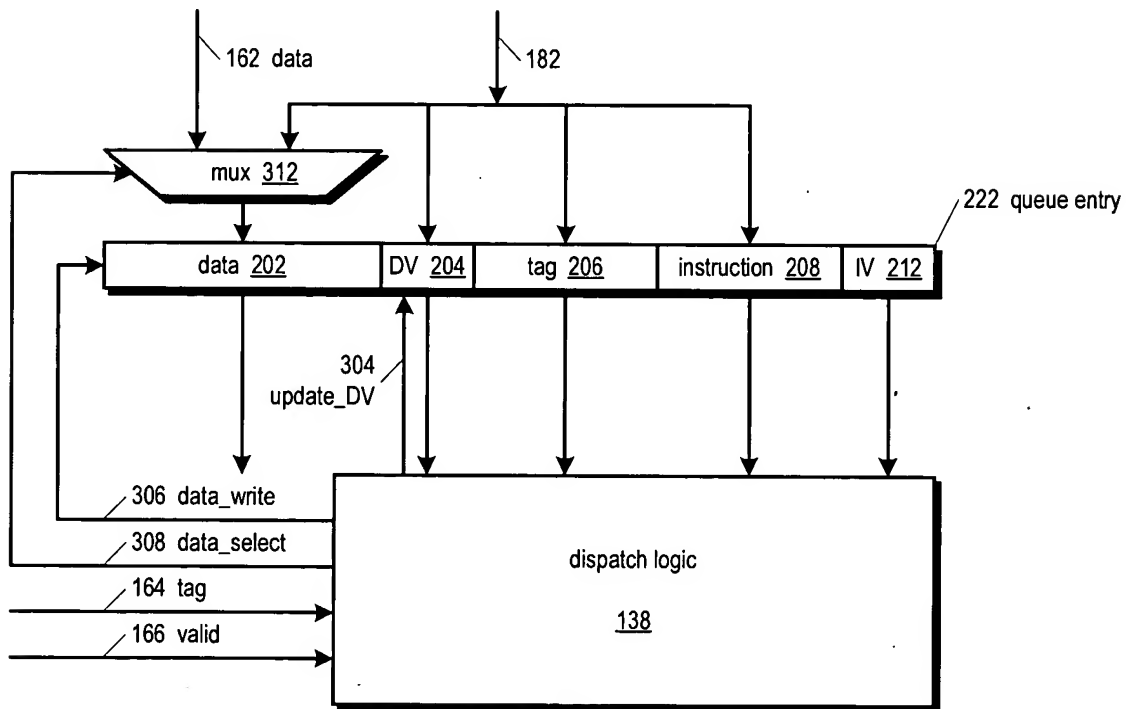
Execution Unit

Fig. 4

Detached Load Operation